AMENDMENTS TO THE SPECIFICATION:

Please replace the section entitled "Description of the Preferred Embodiment," beginning at page 5, with the following amended section (wherein the deletions are shown in strike-out format and the additions are shown with underlining):

Hereinafter, a preferred embodiment of the ~~present~~ invention will be described in more detail referring to the drawings. As used herein, the term "photo process" includes the steps of applying an etching mask, etching, ion implantation, and removal of the etching mask. In addition, the following embodiment is for illustration only, and is not intended to limit the scope of the invention.

Figs. 2a to 2g and Figs. 3a to 3b are sectional views and plane views illustrating a method for aligning a key in a semiconductor device by using an oxide film/silicon dual etching process according to a preferred embodiment of the present invention.

First, as shown in Fig. 2a, an oxide film 120 is deposited on a semiconductor substrate 110 at a thickness of 800 to 1500Å. ~~At this time, t~~The oxide film 120 is used as an anti-etching ~~preventive~~ film during the silicon etching process~~,~~. ~~and, t~~Thus, in the preferred embodiment of the present invention, it is deposited at a thickness of 500 Å above the prior art.

As shown in Fig. 2b, in order to optionally perform a N-well ion implantation in a predetermined region, a N-well photo process is carried out. ~~At this time, conventionally,~~ In conventional applications, a N-well is exposed only to a specific portion of the main chip region 112, and thus no subsequent key formation process for key alignment is performed on the scribe lane region 111. On the other hand, in the preferred embodiment of the present invention, ~~by a method of etching the oxide film 120 using~~ the N-well photo process~~, an align key is formed~~ is used to form a first align key 200 in the scribe lane region 111. Such a scribe region 111 is divided into ~~a~~an area key forming region 114 where ~~a region~~ an area key 210 ~~widely and completely exposed~~ is formed and ~~a~~an area key forming region 113 where ~~a~~an area first align key 200 is formed.

Therefore, according to ~~the~~ a preferred embodiment of the ~~present~~ invention, upon the manufacturing of a N-well reticle, ~~if~~ the two above-mentioned keys are ~~inserted into~~ formed on the scribe lane 111 and ~~as well as~~ a conventional N-well ion

implantation is performed in the N-well ion implantation region 141 of the main chip region 112. ~~By this~~ In this way, the reticle manufacturing process can be carried out without any additional cost.

As shown in Fig. 2c, the oxide film 120 is removed from the area key forming region 114 by a selective etching process using a N-well ion implantation process, to form an area key 210 by completely exposing the silicon surface. ~~At the same time~~Concurrently, a first align key 200, bounded by a step portion of the oxide film, is formed in the first align key forming region 113 ~~due to a step portion of the oxide film by selective etching~~.

According to ~~the~~ a preferred embodiment of the ~~present~~ invention, the area key 210 ~~formed by N-well photo and selective etching methods have a size of~~ has a width of 40μm to 90μm ~~in a forward directional shape~~. ~~On the other hand~~Additionally, the oxide film 120 of the second alignment key 220 forming region of the scribe lane 111 is removed.

Afterwards, a N-well ion implantation process is simultaneously performed on the N-well forming region 141 as well as the portion of ~~main chip region 112 and~~ the scribe lane region 111 ~~with~~in which there is no oxide film 120. However, the key forming region of the scribe lane where the above-mentioned N-well ion implantation is performed is not a portion where a semiconductor device is to be formed, so it is not a matter for concern.

Next, as shown in Fig. 2d, the used N-well photoresist 140 is removed to finish the N-well formation process.

And, as shown in Fig. 2e, after the N-well photo process, a P-well photo process is conducted. At this time, wafer alignment for the P-well photo process is performed by using ~~a~~the first align key 200 ~~formed by a selective etching process using a N-well photo process. Afterwards, in t~~The P-well photo process includes the formation of~~,~~ a second alignment key 220, which allows ~~formation process for~~ subsequent key alignment in, for example, ~~such as~~ a LOCOS photo process~~, etc~~. ~~is performed on the area key forming region 114 along with the P-well forming region of the main chip region 112.~~

~~Continually~~Next, as shown in Figs. 2e and 2f,~~Fig. 2g~~, the P-well forming region 151 of the main chip region 112 is the region where the remaining oxide film

120 ~~remains, in which the oxide film 120 for a subsequent P-well ion implantation~~ is selectively etched to expose the substrate~~silicon~~ wafer 110. ~~At this time~~Concurrently, a P-well photoresist 150 for forming an additional align key 220 exists in the area key forming region 114, and, upon selective etching for a P-well ion implantation, the surface of the substrate~~silicon~~ wafer is etched, instead ~~in stead~~ of etching the oxide film 120.

Therefore, it is possible to make a second align key 220 for conducting the subsequent photo process on the substrate~~silicon~~ surface without ~~any~~ additional steps~~process~~. Afterwards, a P-well is formed by ion implantation in the P-well forming region 151.

Then, as shown in Fig. 2g, ~~a~~the P-well photoresist 150 used in Fig. 2f is removed, ~~to~~ thereby finishing the process. Afterwards, ~~the~~a subsequent photo process such as LOCOS, etc., may be conducted by using the second align key 220 ~~formed in the area key forming region 114~~.

According to ~~the~~ a preferred embodiment of the ~~present~~ invention, the shape of the second align key 220 ~~formed on the scribe lane region 111 upon a P-well formation process~~ is the same as the shape of the first align key 200, thereby enabling mask alignment using the second align key 220 upon a~~the~~ subsequent photo process ~~such as LOCOS, etc~~.

Figs. 3a and 3b ~~to 3c~~ are plane views of align keys formed by the method ~~for aligning a key in a semiconductor device by using an oxide film/silicon dual etching process as~~ shown in Figs. 2a to 2g according to the preferred embodiment of the present invention.

By adapting ~~the~~ this preferred embodiment of the ~~present~~ invention to other semiconductor processes~~every process~~ requiring alignment ~~in a semiconductor process~~, the object of the ~~present~~ invention can be achieved.

As demonstrated ~~seen from~~ above, the ~~present~~ invention can prevent misalignment in a subsequent photo process during a conventional semiconductor key formation process~~, particularly,~~. Specifically, one can employ an oxide film/silicon dual etching process using conventional N-well and P-well reticles ~~and~~ along with conventional processes without any additional reticle manufacturing costs by omitting conventional key photo and etching processes.

Furthermore, it is possible to form an area key and a first alignment key on a scribe lane region at the same time by selectively etching the oxide film that has been deposited on the entire surface of the wafer using a N-well ion implantation mask.

Furthermore, a N-well ion implantation can be performed on the region from which the oxide film is removed ~~from~~ in the same manner as in a conventional semiconductor manufacture process.

Moreover, misalignment can be prevented in a subsequent photo process by forming a second alignment key within an area key~~, whose formation is already finished by removing an oxide film,~~ by using a substrate~~silicon~~ etching method of an oxide film/silicon dual etching using a P-well mask, after~~upon~~ a N-well process, using a P-well ion implantation mask.

Additionally, upon a subsequent photo process, an accurate alignment is enabled by using the second align key formed in the scribe lane even without a photo process using a key reticle.